

What is claimed is:

1. A shift register, comprising:

memory devices formed in a shape of an m-row x n-column matrix and shifting data synchronized with a clock signal;

5 a clock signal delay unit for gradually delaying the clock signal applied to said memory devices starting from an (m)th row memory device that outputs data toward rows of memory device where data are input; and

a data delay unit for delaying the data for a delay time of a clock signal applied to an input side memory device and outputting the result.

2. A shift register according to claim 1, wherein said clock signal delay unit is configured such that delay portions for delaying the clock signal are one-to-one matched to (m-1)th row, (m-2)th row, .. 1st row memory devices, and said delay portions output the clock signal with delay time increased in order of (m-1)th row, (m-2)th row, ... 1st row.

3. A shift register according to claim 2, wherein the delay portions output delay time of t, 2t, ... (m-1)t.

4. A shift register, comprising:

memory devices formed in a shape of an m-row x n-column matrix and shifting data synchronized with a clock signal;

20 a first switching unit that selectively inverts n-bit data in accordance with a first switching control signal and inputs the inverted data to a first row memory device of each column of said memory devices;

a second switching unit that selectively inverts n-bit data shifted by said memory devices and output to each column of (m)th row in accordance with a second switching control signal and outputs the inverted data;

a shift comparing unit that outputs a flag signal while outputting a first switching control signal to said first switching unit when data state of the first row memory devices changes, by utilizing n-bit data being input to said first switching unit and output data of the first row memory device included in said memory devices; and

a shift comparing shift register having m-numbers of memory devices arranged in line and that shifts the flag signal output from said shift comparing unit to be synchronized with shift of said memory devices and outputs a second control signal to said second switching unit.

5. A shift register according to claim 4, wherein said first switching unit and said second switching unit have switching logic corresponding one-to-one to each row of said memory devices, and the switching logic selectively outputs input data and inverted data thereof in accordance with state of the first switching control signal and the second switching control signal.

6. A shift register according to claim 4, wherein said shift comparing unit comprises:

exclusive OR gates for performing exclusive OR sum of n-bit data to be input to said first switching unit and output data of the first row memory device to said memory device, and outputting the result;

a logical combination unit for logically combining outputs of said exclusive OR gates, and outputting a logic high level as said first switching control signal and a flag

signal to be applied to said shift comparing shift register, when a pair of output data and input data of first row memory device is higher than a predetermined number.

7. A shift register according to claim 6, wherein the number determined by said logical combination unit is larger than half of the number of the first row memory device.

8. A driver circuit of liquid crystal display for driving a liquid crystal panel by generating data, gradation voltage, gate voltage, and column/scan control signals in accordance with an image signal input from a predetermined image supply source, the driver circuit having at each unit thereof for processing data, a shift register, the shift register comprising:

memory devices formed in a shape of an m-row x n-column matrix and shifting data as being synchronized data with a clock signal;

a clock signal delay unit for gradually delaying the clock signal applied to said memory devices starting from an (m)th row memory device which outputs data toward rows of memory device when data are input; and

a data delay unit that delays the data for a delay time of a clock signal applied to an input side memory device and outputting the result.

9. A shift register according to claim 8, wherein said clock signal delay unit is configured such that delay portions for delaying the clock signal are one-to-one matched to (m-1)th row, (m-2)th row, .. 1st row memory devices, and said delay portions output the clock signal with delay time increased in order of (m-1)th row, (m-2)th row, ... 1st row.

10. A shift register according to claim 9, wherein the delay portions output delay time of t , $2t$, ... $(m-1)t$.

11. A shift register according to claim 8, wherein the shift register is used in a controller.

12. A shift register according to claim 8, wherein the shift register is used in column driver ICs.

13. A shift register according to claim 8, wherein the shift register is used in scan driver ICs.

14. A shift register in a driver circuit of liquid crystal display for driving a liquid crystal panel by generating data, gradation voltage, gate voltage, and column/scan control signals in accordance with an image signal input from an image source, comprising:

memory devices formed in a shape of an m -row \times n -column matrix and shifting data synchronized with a clock signal;

a first switching unit that selectively inverts n -bit data in accordance with a first switching control signal and inputs the inverted data to a first row memory device of each column of said memory devices;

a second switching unit that selectively inverts n -bit data shifted by said memory devices and output to each column of (m) th row in accordance with a second switching control signal and outputs the inverted data;

a shift comparing unit that outputs a flag signal while outputting a first switching control signal to said first switching unit when data state of the first row memory devices

changes, by utilizing n-bit data being input to said first switching unit and output data of the first row memory device included in said memory device; and

a shift comparing shift register having m-numbers of memory devices arranged in line and that shifts the flag signal output from said shift comparing unit to be
5 synchronized with shift of said memory devices and outputs a second control signal to said second switching unit.

15. A shift register according to claim 14, wherein said first switching unit and said second switching unit have switching logic corresponding one-to-one to each row of said memory devices, and the switching logic selectively outputs input data and inverted data thereof in accordance with state of the first switching control signal and the second switching control signal.

16. A shift register according to claim 14, wherein said shift comparing unit comprises:

exclusive OR gates for performing exclusive OR sum of n-bit data to be input to
15 said first switching unit and output data of the first row memory device to said memory device, and outputting the result;

a logical combination unit for logically combining outputs of said exclusive OR gates, and outputting a logic high level as said first switching control signal and a flag signal to be applied to said shift comparing shift register, when a pair of output data and
20 input data of first row contained in said memory devices is higher than a predetermined number.

17. A shift register according to claim 16, wherein the number determined by

